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Abstract:

[Purpose] Disclosed is a resistor having such a structure that a small amount of heat is generated in a resistive layer of the resistor and that damaging to the resistive layer is avoided when an overload is applied.

[Construction] The resistor of this invention has a dielectric substrate 1, opposing electrodes 2 formed on the dielectric substrate 1, a resistive layer 3 formed between the electrodes 2, and a trimming groove 5 formed in the resistive layer 3. The resistive layer 3 between the electrodes 2 has portions of different thickness. The trimming groove 5 is formed in the portion where the thickness of the resistive layer is larger than that in the portion where the thickness of the resistive layer is the smallest.

Claims:

A resistor comprises a dielectric substrate, opposing electrodes 3 formed on the dielectric substrate, a resistive layer formed between the opposing electrodes, and a trimming groove formed in the resistive layer, wherein the resistive layer between the electrodes has portions of different thickness, and wherein the trimming groove is formed in the portion where the thickness of the resistive layer is larger than that in the portion where the thickness of the resistive layer is the smallest.

Detailed Description

[0001] This invention relates to a resistor and, more particularly, to the shape of a resistive layer of the resistor.

[0002] A conventional chip resistor, as shown in the plan view of Fig. 10 and the cross-sectional view of Fig. 11, generally includes surface electrodes 22 formed at opposing ends of the top surface of a dielectric substrate 21. A resistive layer 23 is formed between the surface electrodes 22. A first protective layer 24 is formed on a part of the surface of the resistive layer 23. A part of the resistive layer 23 and the protective layer 24 is removed to form trimming grooves 25 in the form of notches to adjust the resistance. Thereafter, the resistive layer 23 and the surface electrodes 22 connecting to the resistive layer 23 are covered by a second protective layer 26. Further, a coating layer 27 overlaps with a part of the surface electrodes 22. Further, interior electrodes 28 are formed inside the dielectric substrate 21 at both sides. A side electrode 29 is formed to connect the interior electrode 28 and the surface electrode 22. The interior electrodes 28 and the side electrodes 29 are covered by a coating layer 29 and thus a chip resistor is completed.

[0003] In the above-described conventional chip resistor, the resistive layer 23 between the electrodes 22 generally has a uniform thickness and trimming grooves 25 for adjusting the resistance are formed at random locations of the resistive layer 23. Therefore, after the resistive layer is cut to form the trimming grooves for adjusting the resistance, the cross-sectional area of the remaining portion of the resistive layer becomes too small.

[0004] Therefore, the portion of the resistive layer 23 where the trimming grooves 25 are formed has a high resistance, resulting in high current density and generating a large amount of heat. As a result, when an overload is applied across the electrodes 22 of the chip resistor, the heat generated in the part of the resistive layer 23 where the trimming grooves 25 are formed may not be sufficiently transferred, thereby resulting in a rapid heat generation and damage to the chip resistor.

[0005] Accordingly, an object of this invention is to provide a resistor which is so structured that the resistive layer generates a small amount of heat and that damage to the resistive layer can be avoided even upon application of an overload to the resistor.

[0006] To solve the above-mentioned problems, according to Claim 1 of this invention, a resistor includes a dielectric substrate, opposing electrodes 3 formed on the dielectric substrate, a resistive layer formed between the opposing electrodes, and a trimming groove formed in the resistive layer, wherein the resistive layer between the electrodes has portions of different thickness, and wherein the trimming groove is formed in the portion where the thickness of the resistive layer is larger than that in portions where the thickness of the resistive layer is the smallest.

[0007] In the resistor of this invention, since the trimming groove is formed in a thick portion of the resistive layer, forming the trimming groove to adjust the resistance of the resistive layer will not result in a significant reduction in the cross-sectional area of the resistive layer. Therefore, not only does the resistive layer of the resistor generate a small amount of heat, but that heat generated in the portion of the resistive layer where the trimming groove is formed is reduced, even upon application of an overload, thereby preventing the resistor from being damaged and resulting in a resistor having improved load endurance.

[0008] The resistor according to this invention is now described in detail with reference to the attached figures. Figure 1 is a plan view of the chip resistor in accordance with the first embodiment of this invention wherein surface electrodes 2 are formed at opposing ends of a dielectric substrate 1 made of alumina ceramic. The surface electrodes 2 are formed by printing a silver-containing metal glaze conductive paste, followed by baking. The resistive layer 3 is formed between the opposing surface electrodes 2 in a manner that both ends of the resistive layer 3 overlap with the surface electrodes 2.

[0009] The resistive layer 3 is formed by printing on the substrate 1 a ruthenium-oxide-containing paste, followed by baking so that a flat portion 3a with a uniform thickness is formed between the surface electrodes 2 and that a raised portion 3b is formed anywhere but an area where the resistive layer 3 and the surface electrodes 2 overlap. The raised portion 3b has a thickness greater than that of the flat portion 3a. The surface of the raised portion 3b of the resistive layer 3 is partially or completely covered by a first protective layer 4, which is formed by printing a lead-borosilicate-glass-containing glass glaze series paste, followed by baking. A trimming groove 5 for adjusting the resistance is formed by cutting the first protective layer 4 and the raised portion 3 of the resistive layer 3 by the well-known laser trimming method. Next, epoxy series resin is applied over the resistive layer 3 and a part of the electrodes 2 connecting to the resistive layer 3, and is then cured to form a second protective layer 6. Further, a nickel coating formed from a solder is applied to and overlaps with the surface electrodes 2. Moreover, as shown in Figure 2 showing the cross-sectional view of Figure 1 along line A-A', interior electrodes 8 are formed inside the dielectric substrate 1 at both ends. The interior electrodes 8 are formed by printing a silver-containing metal glaze conductive paste and by baking. Then, side electrodes 9, which are connected to the surface electrodes 2 and the interior electrode 8, are formed at the two side surfaces of the substrate 1 by printing a metal resin series paste followed by curing the same. The interior electrodes 8 and the side electrodes 9 are then covered by a coating layer 7 and the chip resistor is thus completed.

[0010] In this embodiment, a resistive paste is printed by using a screen having a pattern of the flat portion 3a and is then dried. Next, a resistive paste is printed on top of the previously printed paste by using a screen having a pattern of the raised portion and is then dried. Thereafter, the pastes forming the flat portion 3a and the raised portions 3b are baked together to form the raised portion 3b above the flat portion 3a.

[0011] Moreover, in this embodiment, as shown in Figure 3 which shows the cross-section of the flat portion 3a of the resistive layer (along line B-B' of Figure 1), and as shown in Figure 4, which shows the cross-section of the raised portion 3b with a trimming groove formed therein (along line C-C' of Figure 1), comparing the cross-

sectional area of the resistive layer, the portion where the trimming groove is formed has a width half of that of the flat portion and has a thickness about three times that of the flat portion. As a result, the portion where the trimming groove is formed has a cross-sectional area one and a half times that of the flat portion of the resistive layer. Therefore, the portion of the resistive layer where the trimming groove is formed generates almost no heat, and damage to the chip resistor upon application of an overload in a short period of time can be prevented.

[0012] Figure 5 shows a chip resistor according to a second embodiment of this invention. As shown in Figure 6 which shows a part of the cross section of the resistive layer along line a-a' of Figure 5, the second embodiment has substantially the same construction as that of the first embodiment except for the slight wedge shape. In Figure 6, the thickness of the resistive layer 3 is the smallest adjacent to the surface electrode 2 at the right side, and the thickness of the resistive layer 3 increases toward adjacent the surface electrode 2b at the left side of the figure. The trimming groove is formed adjacent to the surface electrode 2b. Then, the area of the resistive layer 3 where the trimming groove to be formed is covered by a first protective layer 4, which is formed by printing a glass glaze series paste containing lead borosilicate glass, followed by backing. A part of the first protective layer 4 and the resistive layer 3 is removed by the well-known laser trimming to form the trimming groove for adjusting the resistance.

[0013] The resistive layer 3 in this embodiment is formed by a typical method shown in Figure 7 which shows the cross-section. This method differs from the embodiment described above in that a screen is placed on the substrate 1 and the resistive layer 3 is formed by applying a resistive paste once. The screen to be used in this method is a mask 11 formed by hardening a UV-hardening resin on the surface of the metallic mesh 10 followed by etching to form the pattern of the resistive layer 3. The mask 11 has a flat section 11a for forming the flat portion of the resistive layer 3 and a column section 11b for forming the slant portion of the resistive layer 3.

[0014] Further, in this embodiment, as shown in Figure 8 which shows the cross-section of the resistive layer 3 having the smallest thickness (along line b-b' of Figure 5), and in figure 9 which shows the cross-section of the area where the trimming groove is formed (along line c-c' of Figure 5), comparing the cross-sectional area of the resistive layer 3, the portion where the trimming grooves are formed has a width half that of the flat portion, and has a thickness 1.7 times larger than that of the flat portion. Because the portion of the resistive layer where the trimming groove is formed has a cross sectional area about 80% larger than that of the flat portion, the area where the trimming groove is formed hardly generates heat, thereby preventing the chip resistor from being damaged even upon application of an overload within a short period of time.

[0015] This invention is not limited to the chip resistor as described in the above embodiments and can also be used in a chip network resistor. Moreover, while the resistor has been shown to have two protective layers applied over the resistive layer, the resistor can have three protective layers. Further, the method of forming the resistive layer is not limited to the thick film method as described above and can include thin film techniques. Moreover, the method of forming the trimming groove is not limited to the laser trimming method and can include methods such as sandblasting.

[0016] Further, the shape of the resistor and the material and the method for forming the resistor of this invention is not limited to the embodiments described above.

Brief Description of Figures

Figure 1 is a plan view of a chip resistor according to the first embodiment of this invention.

Figure 2 is a cross-sectional view of the chip resistor of Figure 1 along line A-A'.

Figure 3 is a cross-sectional view of the chip resistor of Figure 1 along line B-B'.

Figure 4 is a cross-sectional view of the chip resistor of Figure 1 along line C-C'.

Figure 5 is a plan view of a chip resistor according to the second embodiment of this invention.

Figure 6 is a cross-sectional view of the chip resistor of Figure 5 along line a-a'.

Figure 7 is a cross-sectional view of the chip resistor of Figure 5, showing the manufacturing of the resistive layer.

Figure 8 is a cross-sectional view of the chip resistor of Figure 5 along line b-b'.

Figure 9 is a cross-sectional view of the chip resistor of Figure 5 along line c-c'.

Figure 10 is a plan view of a prior art chip resistor.

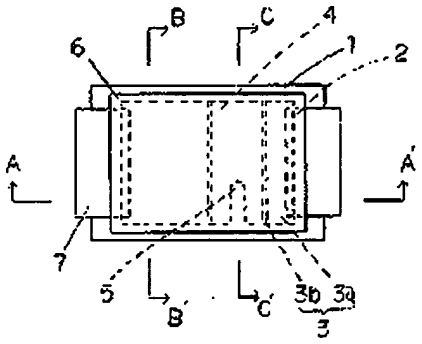
Figure 11 is a cross-sectional view of the prior art chip resistor of Figure 10 along line X-X'.

List of elements

1	substrate
2	surface electrodes
3	resistive layer
4	first protective layer
5	trimming grooves
6	second protective layer
7	coating layer
8	interior electrode
9	side electrode
10	mesh
11	mask

Figures

【図１】



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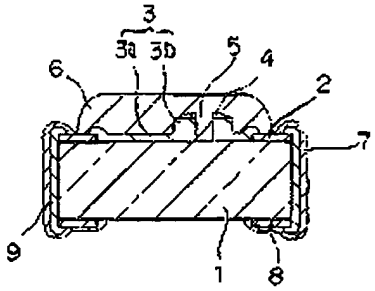

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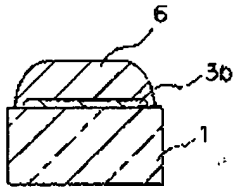

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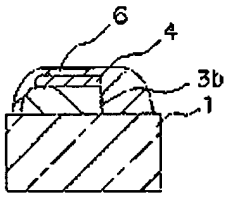

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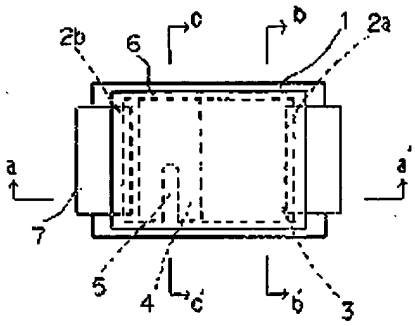

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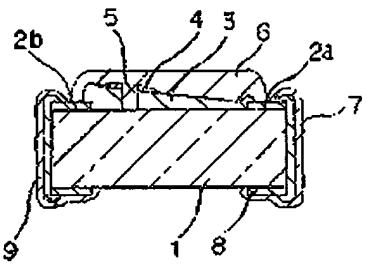

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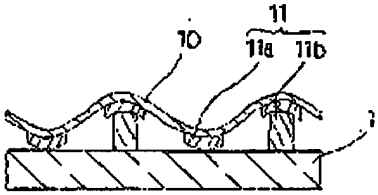

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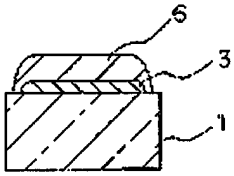

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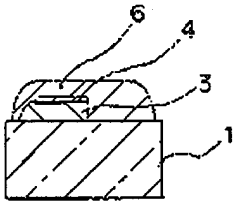

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